ABSTRACT OF THE INVENTION

A method of a bulk tri-gate transistor having stained enhanced mobility and its method of fabrication. The present invention is a nonplanar transistor having a strained enhanced mobility and its method of fabrication. The transistor has a semiconductor body formed on a semiconductor substrate wherein the semiconductor body has a top surface on laterally opposite sidewalls. A semiconductor capping layer is formed on the top surface and on the sidewalls of the semiconductor body. A gate dielectric layer is formed on the semiconductor capping layer on the top surface of a semiconductor body and is formed on the capping layer on the sidewalls of the semiconductor body. A gate electrode having a pair of laterally opposite sidewalls is formed on and around the gate dielectric layer. A pair of source/drain regions are formed in the semiconductor body on opposite sides of the gate electrode.